

	L #	Hits	Search Text	DBs
1	L2	3542	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code)).ab,ti.	USPAT; US-PGPUB
2	L4	14410	(chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address))	USPAT; US-PGPUB
3	L6	2604	execut\$3 near30 4	USPAT; US-PGPUB
4	L8	522	(chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut\$3	EPO; JPO; DERWENT; IBM TDB
5	L9	22638	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 (instruction code)).ab,ti.	EPO; JPO; DERWENT; IBM TDB
6	L10	458	8 and 9	EPO; JPO; DERWENT; IBM TDB
7	L11	5	8 and patch\$3	EPO; JPO; DERWENT; IBM TDB
8	L12	2657	(chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut\$3	USPAT; US-PGPUB
9	L13	3	2 and 12 not 7	USPAT; US-PGPUB
10	L15	423	(chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; JPO; DERWENT; IBM TDB
11	L16	195	(chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; DERWENT; IBM TDB
12	L7	385	2 and 6	USPAT; US-PGPUB
13	L17	187	7 and @pd<19991006	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 59637 41 A	<input type="checkbox"/>	Information processor which rewrites instructions in program to dynamically change program structure and method therefor	717/111
2	US 59637 40 A	<input type="checkbox"/>	System for monitoring computer system performance	717/130
3	US 59499 95 A	<input checked="" type="checkbox"/>	Programmable branch prediction system and method for inserting prediction operation which is independent of execution of program code	712/239
4	US 59481 13 A	<input checked="" type="checkbox"/>	System and method for centrally handling runtime errors	714/38
5	US 59408 59 A	<input checked="" type="checkbox"/>	Emptying packed data state during execution of packed data instructions	711/147
6	US 59405 16 A	<input checked="" type="checkbox"/>	Data security method and system	713/159
7	US 59387 78 A	<input checked="" type="checkbox"/>	System and method for tracing instructions in an information handling system without changing the system source code	714/45
8	US 59371 99 A	<input checked="" type="checkbox"/>	User programmable interrupt mask with timeout for enhanced resource locking efficiency	710/262
9	US 59338 60 A	<input checked="" type="checkbox"/>	Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted	711/213
10	US 59336 26 A	<input checked="" type="checkbox"/>	Apparatus and method for tracing microprocessor instructions	712/227
11	US 59319 57 A	<input checked="" type="checkbox"/>	Support for out-of-order execution of loads and stores in a processor	714/48
12	US 59308 21 A	<input checked="" type="checkbox"/>	Method and apparatus for shared cache lines in split data/code caches	711/146
13	US 59283 58 A	<input checked="" type="checkbox"/>	Information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware	712/239
14	US 59096 98 A	<input checked="" type="checkbox"/>	Cache block store instruction operations where cache coherency is achieved without writing all the way back to main memory	711/145
15	US 59058 81 A	<input checked="" type="checkbox"/>	Delayed state writes for an instruction processor	712/219
16	US 59037 60 A	<input checked="" type="checkbox"/>	Method and apparatus for translating a conditional instruction compatible with a first instruction set architecture (ISA) into a conditional instruction compatible with a second ISA	717/146
17	US 58988 64 A	<input checked="" type="checkbox"/>	Method and system for executing a context-altering instruction without performing a context-synchronization operation within high-performance processors	712/228
18	US 58988 50 A	<input checked="" type="checkbox"/>	Method and system for executing a non-native mode-sensitive instruction within a computer system	712/229
19	US 58954 94 A	<input checked="" type="checkbox"/>	Method of executing perform locked operation instructions for supporting recovery of data consistency if lost due to processor failure, and a method of recovering the data consistency after processor failure	711/150
20	US 58954 86 A	<input checked="" type="checkbox"/>	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121
21	US 58931 57 A	<input checked="" type="checkbox"/>	Blocking symbol control in a computer system to serialize accessing a data resource by simultaneous processor requests	711/150
22	US 58899 83 A	<input checked="" type="checkbox"/>	Compare and exchange operation in a processing system	712/223

	Document ID	U	Title	Current OR
23	US 58753 42 A	<input checked="" type="checkbox"/>	User programmable interrupt mask with timeout	710/260
24	US 58753 18 A	<input checked="" type="checkbox"/>	Apparatus and method of minimizing performance degradation of an instruction set translator due to self-modifying code	716/3
25	US 58621 48 A	<input checked="" type="checkbox"/>	Microcontroller with improved debug capability for internal memory	714/724
26	US 58570 96 A	<input checked="" type="checkbox"/>	Microarchitecture for implementing an instruction to clear the tags of a stack reference register file	712/229
27	US 58451 03 A	<input checked="" type="checkbox"/>	Computer with dynamic instruction reuse	712/216
28	US 58449 86 A	<input checked="" type="checkbox"/>	Secure BIOS	713/187
29	US 58386 94 A	<input checked="" type="checkbox"/>	Dual source data distribution system for integrated circuit tester	714/738
30	US 58359 49 A	<input checked="" type="checkbox"/>	Method of identifying and self-modifying code	711/135
31	US 58357 01 A	<input checked="" type="checkbox"/>	Method and apparatus for modifying relocatable object code files and monitoring programs	714/35
32	US 58290 31 A	<input checked="" type="checkbox"/>	Microprocessor configured to detect a group of instructions and to perform a specific function upon detection	711/137
33	US 58260 73 A	<input checked="" type="checkbox"/>	Self-modifying code handling system	712/226
34	US 58156 99 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/239
35	US 58130 39 A	<input checked="" type="checkbox"/>	Guest execution control system, method and computer process for a virtual machine system	711/156
36	US 58023 38 A	<input checked="" type="checkbox"/>	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
37	US 57969 75 A	<input checked="" type="checkbox"/>	Operand dependency tracking system and method for a processor that executes instructions out of order	712/218
38	US 57908 43 A	<input checked="" type="checkbox"/>	System for modifying microprocessor operations independently of the execution unit upon detection of preselected opcodes	712/226
39	US 57874 80 A	<input checked="" type="checkbox"/>	Lock-up free data sharing	711/148
40	US 57845 52 A	<input checked="" type="checkbox"/>	Debugging a computer program by simulating execution forwards and backwards in a main history log and alternative history logs	714/38
41	US 57817 76 A	<input checked="" type="checkbox"/>	Industrial controller permitting program editing during program execution	717/130
42	US 57650 30 A	<input checked="" type="checkbox"/>	Processor emulator module having a variable pre-fetch queue size for program execution	714/33
43	US 57614 90 A	<input checked="" type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
44	US 57614 68 A	<input checked="" type="checkbox"/>	Hardware mechanism for optimizing instruction and data prefetching by forming augmented prefetch instructions.	712/207

	Document ID	U	Title	Current OR
45	US 57581 83 A	<input checked="" type="checkbox"/>	Method of reducing the number of overhead instructions by modifying the program to locate instructions that access shared data stored at target addresses before program execution	710/5
46	US 57581 15 A	<input checked="" type="checkbox"/>	Interoperability with multiple instruction sets	712/209
47	US 57427 91 A	<input checked="" type="checkbox"/>	Apparatus for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
48	US 57404 42 A	<input checked="" type="checkbox"/>	Method and apparatus for identifying and correcting date calculation errors caused by truncated year values	717/124
49	US 57376 36 A	<input checked="" type="checkbox"/>	Method and system for detecting bypass errors in a load/store unit of a superscalar processor	710/54
50	US 57322 73 A	<input checked="" type="checkbox"/>	System for monitoring compute system performance	717/128
51	US 57322 68 A	<input checked="" type="checkbox"/>	Extended BIOS adapted to establish remote communication for diagnostics and repair	713/2
52	US 57322 54 A	<input checked="" type="checkbox"/>	Pipeline system branch history table storing branch instruction addresses and target addresses with inhibit bits	712/240
53	US 57297 57 A	<input checked="" type="checkbox"/>	Super-computer system architectures using status memory to alter program	712/1
54	US 57245 63 A	<input checked="" type="checkbox"/>	Pipeline processsor	712/233
55	US 57175 87 A	<input checked="" type="checkbox"/>	Method and system for recording noneffective instructions within a data processing system	700/2
56	US 57154 54 A	<input checked="" type="checkbox"/>	Version control of documents by independent line change packaging	707/203
57	US 57015 06 A	<input checked="" type="checkbox"/>	Microcomputer having ROM program which can be altered	712/37
58	US 56921 68 A	<input checked="" type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
59	US 56921 67 A	<input checked="" type="checkbox"/>	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
60	US 56825 28 A	<input checked="" type="checkbox"/>	Spoon-feed initialization in a multiprocessor system	713/1
61	US 56805 97 A	<input checked="" type="checkbox"/>	System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions	712/226
62	US 56712 31 A	<input checked="" type="checkbox"/>	Method and apparatus for performing cache snoop testing on a cache system	714/724
63	US 56689 47 A	<input checked="" type="checkbox"/>	Microprocessor self-test apparatus and method	714/30
64	US 56665 07 A	<input checked="" type="checkbox"/>	Pipelined microinstruction apparatus and methods with branch prediction and speculative state changing	712/218
65	US 56551 32 A	<input checked="" type="checkbox"/>	Register file with multi-tasking support	718/104
66	US 56550 96 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200

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67	US 56528 52 A	<input checked="" type="checkbox"/>	Processor for discriminating between compressed and non-compressed program code, with prefetching, decoding and execution of compressed code in parallel with the decoding, with modified target branch addresses accommodated at run time	712/208
68	US 56491 37 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
69	US 56447 69 A	<input checked="" type="checkbox"/>	System for optimizing program by virtually executing the instruction prior to actual execution of the program to invalidate unnecessary instructions	717/154
70	US 56447 44 A	<input checked="" type="checkbox"/>	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
71	US 56405 26 A	<input checked="" type="checkbox"/>	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
72	US 56363 66 A	<input checked="" type="checkbox"/>	System and method for preserving instruction state-atomicity for translated program	711/163
73	US 56257 87 A	<input checked="" type="checkbox"/>	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
74	US 56196 80 A	<input checked="" type="checkbox"/>	Methods and apparatus for concurrent execution of serial computing instructions using combinatorial architecture for program partitioning	711/173
75	US 56194 08 A	<input checked="" type="checkbox"/>	Method and system for recoding noneffective instructions within a data processing system	712/226
76	US 56130 78 A	<input checked="" type="checkbox"/>	Microprocessor and microprocessor system with changeable effective bus width	710/307
77	US 56025 36 A	<input checked="" type="checkbox"/>	Data synchronization method for use with portable, microprocessor-based device	340/5.2 3
78	US 55967 38 A	<input checked="" type="checkbox"/>	Peripheral device control system using changeable firmware in a single flash memory	711/103
79	US 55948 80 A	<input checked="" type="checkbox"/>	System for executing a plurality of tasks within an instruction in different orders depending upon a conditional value	712/245
80	US 55862 78 A	<input checked="" type="checkbox"/>	Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor	712/235
81	US 55840 27 A	<input checked="" type="checkbox"/>	Method and apparatus for finding induction variables for use in compiling computer instructions	717/160
82	US 55817 20 A	<input checked="" type="checkbox"/>	Apparatus and method for updating information in a microcode instruction	712/226
83	US 55465 54 A	<input checked="" type="checkbox"/>	Apparatus for dynamic register management in a floating point unit	711/203
84	US 55420 84 A	<input checked="" type="checkbox"/>	Method and apparatus for executing an atomic read-modify-write instruction	345/501
85	US 55399 07 A	<input checked="" type="checkbox"/>	System for monitoring computer system performance	717/130
86	US 55353 29 A	<input checked="" type="checkbox"/>	Method and apparatus for modifying relocatable object code files and monitoring programs	714/35
87	US 55220 84 A	<input checked="" type="checkbox"/>	Method and system for invalidating instructions utilizing validity and write delay flags in parallel processing apparatus	712/23
88	US 55112 07 A	<input checked="" type="checkbox"/>	Program control circuit determining the designated number of times a sequence of instructions is repetitively executed to prevent further execution of a jump instruction	712/241

	Document ID	U	Title	Current OR
89	US 55111 75 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
90	US 55049 01 A	<input checked="" type="checkbox"/>	Position independent code location system	717/144
91	US 55048 59 A	<input checked="" type="checkbox"/>	Data processor with enhanced error recovery	714/11
92	US 54796 20 A	<input checked="" type="checkbox"/>	Control unit modifying micro instructions for one cycle execution	712/226
93	US 54653 61 A	<input checked="" type="checkbox"/>	Microcode linker/loader that generates microcode sequences for MRI sequencer by modifying previously generated microcode sequences	717/168
94	US 54637 43 A	<input checked="" type="checkbox"/>	Method of improving SCSI operations by actively patching SCSI processor instructions	710/105
95	US 54541 17 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/23
96	US 54540 75 A	<input checked="" type="checkbox"/>	Device and method for multiple display system having storage means for enlarged images	345/536
97	US 54468 76 A	<input checked="" type="checkbox"/>	Hardware mechanism for instruction/data address tracing	714/47
98	US 54407 04 A	<input checked="" type="checkbox"/>	Data processor having branch predicting function	712/239
99	US 54407 03 A	<input checked="" type="checkbox"/>	System and method for saving state information in a multi-execution unit processor when interruptable instructions are identified	712/228
100	US 54287 86 A	<input checked="" type="checkbox"/>	Branch resolution via backward symbolic execution	717/151
101	US 54189 16 A	<input checked="" type="checkbox"/>	Central processing unit checkpoint retry for store-in and store-through cache systems	712/228
102	US 54086 72 A	<input checked="" type="checkbox"/>	Microcomputer having ROM to store a program and RAM to store changes to the program	712/37
103	US 53922 07 A	<input checked="" type="checkbox"/>	Programmable motion controller with graphical programming aid	700/64
104	US 53597 30 A	<input checked="" type="checkbox"/>	Method of operating a data processing system having a dynamic software update facility	717/169
105	US 53455 67 A	<input checked="" type="checkbox"/>	System and method for modifying program status word system mask, system access key, and address space code with overlap enabled	712/228
106	US 53353 44 A	<input checked="" type="checkbox"/>	Method for inserting new machine instructions into preexisting machine code to monitor preexisting machine access to memory	714/35
107	US 53177 43 A	<input checked="" type="checkbox"/>	System for compiling iterated loops based on the possibility of parallel execution	717/160
108	US 53177 40 A	<input checked="" type="checkbox"/>	Alternate and iterative analysis of computer programs for locating translatable code by resolving callbacks and other conflicting mutual dependencies	717/129
109	US 53033 58 A	<input checked="" type="checkbox"/>	Prefix instruction for modification of a subsequent instruction	712/226
110	US 53013 02 A	<input checked="" type="checkbox"/>	Memory mapping and special write detection in a system and method for simulating a CPU processor	703/20
111	US 53012 95 A	<input checked="" type="checkbox"/>	Data processor apparatus and method with selective caching of instructions	711/125

	Document ID	U	Title	Current OR
112	US 52748 15 A	<input checked="" type="checkbox"/>	Dynamic instruction modifying controller and operation method	712/226
113	US 52690 17 A	<input checked="" type="checkbox"/>	Type 1, 2 and 3 retry and checkpointing	714/15
114	US 52261 32 A	<input checked="" type="checkbox"/>	Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (STO) while using space registers as storage devices for a data processing system	711/209
115	US 52261 30 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
116	US 52147 70 A	<input checked="" type="checkbox"/>	System for flushing instruction-cache only when instruction-cache address and data-cache address are matched and the execution of a return-from-exception-or-interrupt command	711/123
117	US 51971 35 A	<input checked="" type="checkbox"/>	Memory management for scalable compound instruction set machines with in-memory compounding	712/217
118	US 51931 80 A	<input checked="" type="checkbox"/>	System for modifying relocatable object code files to monitor accesses to dynamically allocated memory	717/163
119	US 51858 80 A	<input checked="" type="checkbox"/>	Stored instructions executing type timing signal generating system	713/500
120	US 51685 60 A	<input checked="" type="checkbox"/>	Microprocessor system private split cache tag stores with the system tag store having a different validity bit for the same data line	711/123
121	US 51670 26 A	<input checked="" type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
122	US 51631 46 A	<input checked="" type="checkbox"/>	System responsive to interrupt levels for changing and restoring clock speed by changing and restoring a register value	713/501
123	US 51485 30 A	<input checked="" type="checkbox"/>	Method for reexecuting instruction by altering high bits of instruction address based upon result of a subtraction operation with stored low bits	711/220
124	US 51426 31 A	<input checked="" type="checkbox"/>	System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register	712/217
125	US 51426 30 A	<input checked="" type="checkbox"/>	System for calculating branch destination address based upon address mode bit in operand before executing an instruction which changes the address mode and branching	712/234
126	US 51367 14 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing inter-processor interrupts using shared memory storage in a multi-processor computer system	710/260
127	US 50937 83 A	<input checked="" type="checkbox"/>	Microcomputer register bank accessing	711/220
128	US 50814 62 A	<input checked="" type="checkbox"/>	Method of deriving phase of pseudo-random code signal in global positioning system receiver	342/352
129	US 50382 80 A	<input checked="" type="checkbox"/>	Information processing apparatus having address expansion function	712/237
130	US 49929 77 A	<input checked="" type="checkbox"/>	Cache memory device constituting a memory device used in a computer	711/143
131	US 49823 58 A	<input checked="" type="checkbox"/>	High speed programmable controller for executing an instruction formed by a ladder	345/467
132	US 49706 79 A	<input checked="" type="checkbox"/>	Pulse input apparatus	341/122
133	US 49624 63 A	<input checked="" type="checkbox"/>	Video imaging device with image altering controls and related method	715/500 .1

	Document ID	U	Title	Current OR
134	US 49586 32 A	<input checked="" type="checkbox"/>	Adaptable, digital computer controlled cardiac pacemaker	607/11
135	US 49145 84 A	<input checked="" type="checkbox"/>	Rules and apparatus for an intermediate code memory that buffers code segments	712/237
136	US 48796 46 A	<input checked="" type="checkbox"/>	Data processing system with a pipelined structure for editing trace memory contents and tracing operations during system debugging	712/227
137	US 48356 79 A	<input checked="" type="checkbox"/>	Microprogram control system	712/212
138	US 48253 60 A	<input checked="" type="checkbox"/>	System and method for parallel processing with mostly functional languages	718/106
139	US 48253 55 A	<input checked="" type="checkbox"/>	Instruction format for program control type data processing systems	712/224
140	US 47945 22 A	<input checked="" type="checkbox"/>	Method for detecting modified object code in an emulator	703/26
141	US 47929 96 A	<input checked="" type="checkbox"/>	Information medium for communicating data and/or a selectable control transfer program between the medium end and external device	398/140
142	US 47665 38 A	<input checked="" type="checkbox"/>	Microprocessor having variable data width	710/307
143	US 47605 19 A	<input checked="" type="checkbox"/>	Data processing apparatus and method employing collision detection and prediction	712/217
144	US 47424 66 A	<input checked="" type="checkbox"/>	System for measuring path coverage represented by the degree of passage of execution paths in a program	714/45
145	US 47317 42 A	<input checked="" type="checkbox"/>	Video display control system	345/572
146	US 46758 10 A	<input checked="" type="checkbox"/>	Digital data processing system having a uniquely organized memory system using object-based addressing and in which operand data is identified by names accessed by name tables	711/202
147	US 46384 52 A	<input checked="" type="checkbox"/>	Programmable controller with dynamically altered programmable real time interrupt interval	710/266
148	US 46369 41 A	<input checked="" type="checkbox"/>	Method and apparatus for analysis of microprocessor operation	714/25
149	US 46252 94 A	<input checked="" type="checkbox"/>	Table-driven apparatus for data display and modification	715/530
150	US 46112 81 A	<input checked="" type="checkbox"/>	Apparatus for analyzing microprocessor operation	714/39
151	US 46023 47 A	<input checked="" type="checkbox"/>	Microcomputer addressing system and electronic timepiece utilizing the same	702/178
152	US 45846 40 A	<input checked="" type="checkbox"/>	Method and apparatus for a compare and swap instruction	707/200
153	US 45584 11 A	<input checked="" type="checkbox"/>	Polymorphic programmable units employing plural levels of sub-instruction sets	712/37
154	US 45382 25 A	<input checked="" type="checkbox"/>	Table-driven apparatus for data display and modification	715/530
155	US 45162 03 A	<input checked="" type="checkbox"/>	Improved apparatus for encaching data whose value does not change during execution of an instruction sequence	711/3
156	US 45009 59 A	<input checked="" type="checkbox"/>	Apparatus for invalidating the content of an instruction buffer by program store compare check	712/207

	Document ID	U	Title	Current OR
157	US 44941 14 A	<input checked="" type="checkbox"/>	Security arrangement for and method of rendering microprocessor-controlled electronic equipment inoperative after occurrence of disabling event	340/5.3 1
158	US 44660 57 A	<input checked="" type="checkbox"/>	Digital data processing system responsive to instructions containing operation code modifiers	712/210
159	US 44596 64 A	<input checked="" type="checkbox"/>	Multiprocessor computer system with dynamic allocation of multiprocessing tasks and processor for use in such multiprocessor computer system	718/105
160	US 44545 79 A	<input checked="" type="checkbox"/>	System for performing call and return operations	712/242
161	US 44491 85 A	<input checked="" type="checkbox"/>	Implementation of instruction for a branch which can cross one page boundary	712/234
162	US 44398 30 A	<input checked="" type="checkbox"/>	Computer system key and lock protection mechanism	711/164
163	US 44344 64 A	<input checked="" type="checkbox"/>	Memory protection system for effecting alteration of protection information without intervention of control program	711/164
164	US 44109 59 A	<input checked="" type="checkbox"/>	Computer control system for selecting a desired control program from a plurality of control programs	187/247
165	US 44096 54 A	<input checked="" type="checkbox"/>	Data processor adapted for interruption to an instruction stream	711/213
166	US 43542 31 A	<input checked="" type="checkbox"/>	Apparatus for reducing the instruction execution time in a computer employing indirect addressing of a data memory	711/220
167	US 43162 45 A	<input checked="" type="checkbox"/>	Apparatus and method for semaphore initialization in a multiprocessing computer system for process synchronization	718/106
168	US 43153 14 A	<input checked="" type="checkbox"/>	Priority vectored interrupt having means to supply branch address directly	712/244
169	US 43062 85 A	<input checked="" type="checkbox"/>	Data processing apparatus	712/226
170	US 42875 61 A	<input checked="" type="checkbox"/>	Address formulation interlock mechanism	712/217
171	US 42505 45 A	<input checked="" type="checkbox"/>	Data processing apparatus providing autoloading of memory pointer registers	712/208
172	US 42401 42 A	<input checked="" type="checkbox"/>	Data processing apparatus providing autoincrementing of memory pointer registers	712/42
173	US 41953 39 A	<input checked="" type="checkbox"/>	Sequential control system	712/234
174	US 41842 01 A	<input checked="" type="checkbox"/>	Integrating processor element	710/36
175	US 41033 26 A	<input checked="" type="checkbox"/>	Time-slicing method and apparatus for disk drive	718/107
176	US 40952 78 A	<input checked="" type="checkbox"/>	Instruction altering system	712/226
177	US 39848 13 A	<input checked="" type="checkbox"/>	Microprocessor system	712/40
178	US 39835 41 A	<input checked="" type="checkbox"/>	Polymorphic programmable units employing plural levels of phased sub-instruction sets	712/247
179	US 39835 39 A	<input checked="" type="checkbox"/>	Polymorphic programmable units employing plural levels of sub-instruction sets	712/247

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180	US 39597 77 A	<input checked="" type="checkbox"/>	Data processor for pattern recognition and the like	712/234
181	US 38270 29 A	<input checked="" type="checkbox"/>	MEMORY AND PROGRAM PROTECTION SYSTEM FOR A DIGITAL COMPUTER SYSTEM	711/163
182	US 37818 23 A	<input checked="" type="checkbox"/>	COMPUTER CONTROL UNIT CAPABLE OF DYNAMICALLY REINTERPRETING INSTRUCTIONS	712/209
183	US 37787 75 A	<input checked="" type="checkbox"/>	MICROPROGRAMMED TERMINAL	712/245
184	US 37649 88 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSING DEVICE USING ADVANCED CONTROL SYSTEM	712/234
185	US 37378 67 A	<input checked="" type="checkbox"/>	DIGITAL COMPUTER WITH ACCUMULATOR SIGN BIT INDEXING	712/226
186	US 37189 12 A	<input checked="" type="checkbox"/>	INSTRUCTION EXECUTION UNIT	712/217
187	US 35977 39 A	<input checked="" type="checkbox"/>	METHOD FOR OPERATING A DATA PROCESSOR	711/200

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1	L2	3542	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code)).ab,ti.	USPAT; US-PGPUB
2	L4	14410	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address))	USPAT; US-PGPUB
3	L6	2604	execut\$3 near30 4	USPAT; US-PGPUB
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11	L16	195	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; DERWENT; IBM_TDB
12	L7	385	2 and 6	USPAT; US-PGPUB
13	L17	187	7 and @pd<19991006	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	WO 98546 39 A1	<input type="checkbox"/>	PATCHING APPARATUS AND METHOD FOR UPGRADING MODEM SOFTWARE CODE	
2	US 66913 08 B	<input type="checkbox"/>	Hot patch circuit for changing micro code to be executed in processor, has cache system that selectively compares, for each address generated by program counter, generated address to addresses stored in cache system	
3	US 20030 02875 7 A	<input type="checkbox"/>	Instructions modifying method for uniprocessor system, involves overwriting memory location with value representing patch class instruction concurrent with execution of another value representing patch class instruction	
4	EP 12800 56 A	<input type="checkbox"/>	Linking object code modules to form executable program by deriving call frame information instructions from call frame information macros	
5	US 63178 70 B	<input type="checkbox"/>	Inter-module procedure call optimization for computer program, involves modifying call instruction to directly call unresolved module at determined location, once unresolved module is called during program execution	

	Document ID	U	Title	Current OR
1	US 20040 06471 5 A1	<input type="checkbox"/>	Method and device for accessing a memory to prevent tampering of a program in the memory	713/193
2	US 20040 06468 5 A1	<input checked="" type="checkbox"/>	System and method for real-time tracing and profiling of a superscalar processor implementing conditional execution	712/227
3	US 20040 05970 6 A1	<input checked="" type="checkbox"/>	System and method for providing concurrent usage and replacement of non-native language codes	707/1
4	US 20040 04977 0 A1	<input checked="" type="checkbox"/>	Infrastructure for generating a downloadable, secure runtime binary image for a secondary processor	717/162
5	US 20040 04966 3 A1	<input checked="" type="checkbox"/>	System with wide operand architecture and method	712/222
6	US 20040 04965 4 A1	<input checked="" type="checkbox"/>	Secondary processor execution kernel framework	712/35
7	US 20040 04501 8 A1	<input checked="" type="checkbox"/>	Using address space bridge in postoptimizer to route indirect calls at runtime	719/331
8	US 20040 03484 5 A1	<input checked="" type="checkbox"/>	Code conversion method and apparatus	717/100
9	US 20040 03095 3 A1	<input checked="" type="checkbox"/>	Fault-tolerant architecture for in-circuit programming	714/10
10	US 20040 01988 6 A1	<input checked="" type="checkbox"/>	Compilation of application code in a data processing apparatus	717/158
11	US 20040 01977 0 A1	<input checked="" type="checkbox"/>	Optimization apparatus, compiler program, optimization method and recording medium	712/227
12	US 20040 01592 2 A1	<input checked="" type="checkbox"/>	Program preparation apparatus	717/154
13	US 20040 01567 5 A1	<input checked="" type="checkbox"/>	SMC detection and reverse translation in a translation lookaside buffer	711/207
14	US 20030 23338 6 A1	<input checked="" type="checkbox"/>	High speed virtual machine and compiler	718/100
15	US 20030 22977 7 A1	<input checked="" type="checkbox"/>	Use of hashing in a secure boot loader	713/2
16	US 20030 22599 3 A1	<input checked="" type="checkbox"/>	Computer system	711/202
17	US 20030 21298 3 A1	<input checked="" type="checkbox"/>	Method and system for modifying executable code to add additional functionality	717/110

	Document ID	U	Title	Current OR
18	US 20030 20470 5 A1	<input checked="" type="checkbox"/>	Prediction of branch instructions in a data processing apparatus	712/207
19	US 20030 20467 3 A1	<input checked="" type="checkbox"/>	Data prefetching apparatus in a data processing system and method therefor	711/137
20	US 20030 19179 2 A1	<input checked="" type="checkbox"/>	High speed virtual machine and compiler	718/100
21	US 20030 15901 9 A1	<input checked="" type="checkbox"/>	Prediction of instructions in a data processing apparatus	712/207
22	US 20030 14033 8 A1	<input checked="" type="checkbox"/>	Method, apparatus and article for generation of debugging information	717/162
23	US 20030 14022 2 A1	<input checked="" type="checkbox"/>	System for managing circuitry of variable function information processing circuit and method for managing circuitry of variable function information processing circuit	713/1
24	US 20030 10129 2 A1	<input checked="" type="checkbox"/>	System and method for isolating applications from each other	719/328
25	US 20030 09755 1 A1	<input checked="" type="checkbox"/>	System and method for deploying a hardware configuration with a computer program	713/1
26	US 20030 09738 2 A1	<input checked="" type="checkbox"/>	Identifying changed records in a file stored on an electronic token	707/204
27	US 20030 08443 3 A1	<input checked="" type="checkbox"/>	Profile-guided stride prefetching	717/158
28	US 20030 08422 9 A1	<input checked="" type="checkbox"/>	Methods and apparatus for modifying programs stored in read only memory	711/102
29	US 20030 08408 9 A1	<input checked="" type="checkbox"/>	Data transfer apparatus	709/200
30	US 20030 04666 2 A1	<input checked="" type="checkbox"/>	Data reproduction apparatus	717/115
31	US 20030 04649 4 A1	<input checked="" type="checkbox"/>	Program control flow conditioned on presence of requested data in cache memory	711/138
32	US 20030 04122 5 A1	<input checked="" type="checkbox"/>	Mechanism for handling load lock/store conditional primitives in directory-based distributed shared memory multiprocessors	712/30
33	US 20030 03722 3 A1	<input checked="" type="checkbox"/>	Apparatus and method for ownership load locked misses for atomic lock acquisition in a multiprocessor computer system	712/28
34	US 20030 03359 2 A1	<input checked="" type="checkbox"/>	Software debugger and software development support system	717/128

	Document ID	U	Title	Current OR
35	US 20030 02875 7 A1	<input checked="" type="checkbox"/>	Concurrent modification and execution of instructions	712/226
36	US 20030 02396 4 A1	<input checked="" type="checkbox"/>	System and method for compacting field upgradeable wireless communication device software code sections	717/172
37	US 20030 01890 6 A1	<input checked="" type="checkbox"/>	Method and system for protecting software applications against static and dynamic software piracy techniques	713/189
38	US 20020 19906 7 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
39	US 20020 19454 5 A1	<input checked="" type="checkbox"/>	Method of testing embedded memory array and embedded memory controller for use therewith	714/42
40	US 20020 19445 4 A1	<input checked="" type="checkbox"/>	Method and arrangement for instruction word generation in the driving of functional units in a processor	712/24
41	US 20020 18439 9 A1	<input checked="" type="checkbox"/>	Interpreting functions utilizing a hybrid of virtual and native machine instructions	719/310
42	US 20020 18417 9 A1	<input checked="" type="checkbox"/>	Method and system for distributing product information	707/1
43	US 20020 17208 2 A1	<input checked="" type="checkbox"/>	Method and apparatus for changing region code of digital versatile disc drive	365/200
44	US 20020 16393 5 A1	<input checked="" type="checkbox"/>	System and method for providing transformation of multi-protocol packets in a data stream	370/466
45	US 20020 15704 2 A1	<input checked="" type="checkbox"/>	Algorithmically programmable memory tester with breakpoint trigger, error jamming and 'scope mode that memorizes target sequences	714/45
46	US 20020 14790 1 A1	<input checked="" type="checkbox"/>	Method of handling instructions within a processor with decoupled architecture, in particular a processor for digital signal processing, and corresponding processor	712/225
47	US 20020 14424 5 A1	<input checked="" type="checkbox"/>	Static compilation of instrumentation code for debugging support	717/140
48	US 20020 14424 1 A1	<input checked="" type="checkbox"/>	Debugging support using dynamic re-compilation	717/136
49	US 20020 12415 8 A1	<input checked="" type="checkbox"/>	Virtual r0 register	712/226
50	US 20020 12092 3 A1	<input checked="" type="checkbox"/>	Method for software pipelining of irregular conditional control loops	717/160
51	US 20020 11666 3 A1	<input checked="" type="checkbox"/>	Data processing system with on-chip FIFO for storing debug information and method therefor	714/30

	Document ID	U	Title	Current OR
52	US 20020 11659 7 A1	<input checked="" type="checkbox"/>	Memory accelerator for ARM processors	712/207
53	US 20020 11214 9 A1	<input checked="" type="checkbox"/>	Data processor and method of operation	712/236
54	US 20020 10407 7 A1	<input checked="" type="checkbox"/>	Multi-threaded fragment patching	717/162
55	US 20020 10002 8 A1	<input checked="" type="checkbox"/>	System for modifying the functionality of compiled computer code at run-time	717/139
56	US 20020 09357 4 A1	<input checked="" type="checkbox"/>	Digital camera	348/231 .6
57	US 20020 09196 3 A1	<input checked="" type="checkbox"/>	Fault-tolerant architecture for in-circuit programming	714/2
58	US 20020 08792 5 A1	<input checked="" type="checkbox"/>	Computer processor read/alter/rewrite optimization cache invalidate signals	714/718
59	US 20020 08784 6 A1	<input checked="" type="checkbox"/>	Reconfigurable processing system and method	712/229
60	US 20020 08781 0 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
61	US 20020 07339 8 A1	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR MODIFYING EXECUTABLE CODE TO ADD ADDITIONAL FUNCTIONALITY	717/110
62	US 20020 06691 0 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit	257/200
63	US 20020 06247 9 A1	<input checked="" type="checkbox"/>	Microcontroller with modifiable program	717/168
64	US 20020 04986 5 A1	<input checked="" type="checkbox"/>	Direct invocation of methods using class loader	719/315
65	US 20020 04629 8 A1	<input checked="" type="checkbox"/>	INTERPRETING FUNCTIONS UTILIZING A HYBRID OF VIRTUAL AND NATIVE MACHINE INSTRUCTIONS	719/310
66	US 20020 03287 9 A1	<input checked="" type="checkbox"/>	Fault-tolerant architecture for in-circuit programming	714/2
67	US 20020 02935 7 A1	<input checked="" type="checkbox"/>	Method and system of memory management using stack walking	714/9
68	US 20020 00489 7 A1	<input checked="" type="checkbox"/>	Data processing apparatus for executing multiple instruction sets	712/227

	Document ID	U	Title	Current OR
69	US 20020 00257 3 A1	<input checked="" type="checkbox"/>	Processor with reconfigurable arithmetic data path	708/501
70	US 20010 04746 9 A1	<input checked="" type="checkbox"/>	Emptying packed data state during execution of packed data instructions	712/229
71	US 20010 03749 7 A1	<input checked="" type="checkbox"/>	Apparatus and method for generating optimization objects	717/160
72	US 20010 02753 8 A1	<input checked="" type="checkbox"/>	Computer register watch	714/28
73	US 20010 02533 8 A1	<input checked="" type="checkbox"/>	Systems and methods for transient error recovery in reduced instruction set computer processors via instruction retry	712/228
74	US 20010 02097 8 A1	<input checked="" type="checkbox"/>	Electronic camera	348/222 .1
75	US 20010 00712 4 A1	<input checked="" type="checkbox"/>	Program modification device	711/165
76	US 20010 00475 7 A1	<input checked="" type="checkbox"/>	Processor and method of controlling the same	712/218
77	US 67185 45 B1	<input checked="" type="checkbox"/>	Apparatus for managing resources of a signal processor, a resource managing program transferring method and recording medium	717/168
78	US 67150 51 B2	<input checked="" type="checkbox"/>	Program modification device	711/165
79	US 67049 25 B1	<input checked="" type="checkbox"/>	Dynamic binary translator with a system and method for updating and maintaining coherency of a translation cache	717/138
80	US 66912 46 B1	<input checked="" type="checkbox"/>	System and method of processing partially defective memories	714/8
81	US 66869 04 B1	<input checked="" type="checkbox"/>	Wheel reporting method for a personal computer keyboard interface	345/168
82	US 66788 86 B2	<input checked="" type="checkbox"/>	Apparatus and method for generating optimization objects	717/151
83	US 66752 98 B1	<input checked="" type="checkbox"/>	Execution of instructions using op code lengths longer than standard op code lengths to encode data	713/190
84	US 66717 98 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/234
85	US 66683 72 B1	<input checked="" type="checkbox"/>	Software profiling method and apparatus	717/130
86	US 66614 18 B1	<input checked="" type="checkbox"/>	Character animation system	345/473
87	US 66473 01 B1	<input checked="" type="checkbox"/>	Process control system with integrated safety control system	700/79
88	US 66369 50 B1	<input checked="" type="checkbox"/>	Computer architecture for shared memory access	711/147

	Document ID	U	Title	Current OR
89	US 66292 41 B1	<input checked="" type="checkbox"/>	Data processing apparatus with non-volatile memory for both program and data	713/100
90	US 66292 09 B1	<input checked="" type="checkbox"/>	Cache coherency protocol permitting sharing of a locked data granule	711/141
91	US 66257 01 B1	<input checked="" type="checkbox"/>	Extended cache coherency protocol with a modified store instruction lock release indicator	711/152
92	US 66188 24 B1	<input checked="" type="checkbox"/>	Method and apparatus for modifying relocatable object code files and monitoring programs	714/35
93	US 66163 58 B1	<input checked="" type="checkbox"/>	Keyboard structure alteration method	400/472
94	US 66153 33 B1	<input checked="" type="checkbox"/>	Data processing device, method of executing a program and method of compiling	711/169
95	US 66153 04 B1	<input checked="" type="checkbox"/>	Processing unit in which access to system memory is controlled	710/260
96	US 66119 00 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
97	US 65981 66 B1	<input checked="" type="checkbox"/>	Microprocessor in which logic changes during execution	713/190
98	US 65948 21 B1	<input checked="" type="checkbox"/>	Translation consistency checking for modified target instructions by comparing to original copy	717/136
99	US 65947 34 B1	<input checked="" type="checkbox"/>	Method and apparatus for self modifying code detection using a translation lookaside buffer	711/146
100	US 65713 29 B1	<input checked="" type="checkbox"/>	Detection of overwrite modification by preceding instruction possibility of fetched instruction code using fetched instructions counter and store target address	712/205
101	US 65606 41 B1	<input checked="" type="checkbox"/>	System, method, and adapter card for remote console emulation including remote control of a peripheral device	709/219
102	US 65395 00 B1	<input checked="" type="checkbox"/>	System and method for tracing	714/45
103	US 65360 34 B1	<input checked="" type="checkbox"/>	Method for modifying code sequences and related device	717/110
104	US 65230 95 B1	<input checked="" type="checkbox"/>	Method and data processing system for using quick decode instructions	711/144
105	US 65131 56 B2	<input checked="" type="checkbox"/>	Interpreting functions utilizing a hybrid of virtual and native machine instructions	717/151
106	US 65103 51 B1	<input checked="" type="checkbox"/>	Modifier function blocks in a process control system	700/18
107	US 65052 95 B1	<input checked="" type="checkbox"/>	Data processor	712/241
108	US 65021 76 B1	<input checked="" type="checkbox"/>	Computer system and methods for loading and modifying a control program without stopping the computer system using reserve areas	711/170
109	US 64670 84 B1	<input checked="" type="checkbox"/>	Systems and methods for reprogramming an embedded device with program code using relocatable program code	717/136
110	US 64635 11 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
111	US 64250 74 B1	<input checked="" type="checkbox"/>	Method and apparatus for rapid execution of FCOM and FSTSW	712/222

	Document ID	U	Title	Current OR
112	US 64185 14 B1	<input checked="" type="checkbox"/>	Removal of posted operations from cache operations queue	711/133
113	US 64153 60 B1	<input checked="" type="checkbox"/>	Minimizing self-modifying code checks for uncacheable memory types	711/139
114	US 64053 16 B1	<input checked="" type="checkbox"/>	Method and system for injecting new code into existing application code	713/190
115	US 64053 07 B1	<input checked="" type="checkbox"/>	Apparatus and method for detecting and handling self-modifying code conflicts in an instruction fetch pipeline	712/239
116	US 64012 21 B1	<input checked="" type="checkbox"/>	Fault-tolerant architecture for in-circuit programming	714/36
117	US 64011 96 B1	<input checked="" type="checkbox"/>	Data processor system having branch control and method thereof	712/241
118	US 63935 56 B1	<input checked="" type="checkbox"/>	Apparatus and method to change processor privilege without pipeline flush	712/229
119	US 63895 12 B1	<input checked="" type="checkbox"/>	Microprocessor configured to detect updates to instructions outstanding within an instruction processing pipeline and computer system including same	711/125
120	US 63828 46 B1	<input checked="" type="checkbox"/>	Intermediate instruction execution processor which resolves symbolic references without modifying intermediate instruction code	712/209
121	US 63816 79 B1	<input checked="" type="checkbox"/>	Information processing system with prefetch instructions having indicator bits specifying cache levels for prefetching	711/137
122	US 63743 33 B1	<input checked="" type="checkbox"/>	Cache coherency protocol in which a load instruction hint bit is employed to indicate deallocation of a modified cache line supplied by intervention	711/145
123	US 63603 18 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
124	US 63601 94 B1	<input checked="" type="checkbox"/>	Different word size multiprocessor emulation	703/26
125	US 63569 18 B1	<input checked="" type="checkbox"/>	Method and system for managing registers in a data processing system supports out-of-order and speculative instruction execution	707/203
126	US 63473 61 B1	<input checked="" type="checkbox"/>	Cache coherency protocols with posted operations	711/141
127	US 63453 40 B1	<input checked="" type="checkbox"/>	Cache coherency protocol with ambiguous state for posted operations	711/141
128	US 63432 80 B1	<input checked="" type="checkbox"/>	Distributed execution software license server	705/55
129	US 63395 60 B1	<input checked="" type="checkbox"/>	Semiconductor memory based on address transitions	365/233 .5
130	US 63362 12 B1	<input checked="" type="checkbox"/>	Self modifying code to test all possible addressing modes	717/124
131	US 63306 43 B1	<input checked="" type="checkbox"/>	Cache coherency protocols with global and local posted operations	711/141
132	US 63178 70 B1	<input checked="" type="checkbox"/>	System and method for optimization of inter-module procedure calls	717/151
133	US 63178 68 B1	<input checked="" type="checkbox"/>	Process for transparently enforcing protection domains and access control as well as auditing operations in software components	717/127
134	US 63082 61 B1	<input checked="" type="checkbox"/>	Computer system having an instruction for probing memory latency	712/219

	Document ID	U	Title	Current OR
135	US 62984 81 B1	<input checked="" type="checkbox"/>	System for modifying the functionality of compiled computer code at run-time	717/110
136	US 62859 74 B1	<input checked="" type="checkbox"/>	Hardware verification tool for multiprocessors	703/13
137	US 62826 75 B1	<input checked="" type="checkbox"/>	Fault-tolerant architecture for in-circuit programming	714/36
138	US 62826 39 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
139	US 62666 86 B1	<input checked="" type="checkbox"/>	Emptying packed data state during execution of packed data instructions	708/204
140	US 62567 77 B1	<input checked="" type="checkbox"/>	Method and apparatus for debugging of optimized machine code, using hidden breakpoints	717/129
141	US 62499 06 B1	<input checked="" type="checkbox"/>	Adaptive method and system to minimize the effect of long table walks	717/153
142	US 62471 18 B1	<input checked="" type="checkbox"/>	Systems and methods for transient error recovery in reduced instruction set computer processors via instruction retry	712/228
143	US 62470 36 B1	<input checked="" type="checkbox"/>	Processor with reconfigurable arithmetic data path	708/603
144	US 62405 46 B1	<input checked="" type="checkbox"/>	Identifying date fields for runtime year 2000 system solution process, method and article of manufacture	717/131
145	US 62405 06 B1	<input checked="" type="checkbox"/>	Expanding instructions with variable-length operands to a fixed length	712/213
146	US 62370 88 B1	<input checked="" type="checkbox"/>	System and method for tracking in-flight instructions in a pipeline	712/239
147	US 62370 76 B1	<input checked="" type="checkbox"/>	Method for register renaming by copying a 32 bits instruction directly or indirectly to a 64 bits instruction	712/23
148	US 62065 84 B1	<input checked="" type="checkbox"/>	Method and apparatus for modifying relocatable object code files and monitoring programs	714/35
149	US 61991 39 B1	<input checked="" type="checkbox"/>	Refresh period control apparatus and method, and computer	711/106
150	US 61957 56 B1	<input checked="" type="checkbox"/>	Power reduction for multiple-instruction-word processors by modification of instruction words	713/340
151	US 61925 17 B1	<input checked="" type="checkbox"/>	Method, apparatus, and product for improved garbage collection in a memory system through the removal of reference conflicts	717/154
152	US 61856 74 B1	<input checked="" type="checkbox"/>	Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor	712/230
153	US 61785 49 B1	<input checked="" type="checkbox"/>	Memory writer with deflective memory-cell handling capability	717/124
154	US 61784 84 B1	<input checked="" type="checkbox"/>	DCBST with ICBI mechanism to maintain coherency of bifurcated data and instruction caches	711/145
155	US 61734 21 B1	<input checked="" type="checkbox"/>	Centrally handling runtime errors	714/38
156	US 61700 82 B1	<input checked="" type="checkbox"/>	Taking corrective action in computer programs during instruction processing	717/127
157	US 61450 59 A	<input checked="" type="checkbox"/>	Cache coherency protocols with posted operations and tagged coherency states	711/143

	Document ID	U	Title	Current OR
158	US 61417 68 A	<input checked="" type="checkbox"/>	Self-corrective memory system and method	714/8
159	US 61416 98 A	<input checked="" type="checkbox"/>	Method and system for injecting new code into existing application code	719/331
160	US 61380 59 A	<input checked="" type="checkbox"/>	Vehicle control system and unit for preventing power supply cutoff during re-programming mode	701/1
161	US 61356 51 A	<input checked="" type="checkbox"/>	Patching apparatus and method for upgrading modem software code	717/168
162	US 61311 45 A	<input checked="" type="checkbox"/>	Information processing unit and method for controlling a hierarchical cache utilizing indicator bits to control content of prefetching operations	711/137
163	US 61287 71 A	<input checked="" type="checkbox"/>	System and method for automatically modifying database access methods to insert database object handling instructions	717/111
164	US 61287 27 A	<input checked="" type="checkbox"/>	Self modifying code to test all possible addressing modes	712/227
165	US 61287 10 A	<input checked="" type="checkbox"/>	Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system	711/152
166	US 61184 49 A	<input checked="" type="checkbox"/>	Server system and method for modifying a cursor image	345/861
167	US 61122 80 A	<input checked="" type="checkbox"/>	Method and apparatus for distinct instruction pointer storage in a partitioned cache memory	711/129
168	US 61087 97 A	<input checked="" type="checkbox"/>	Method and system for loading microprograms in partially defective memory	714/8
169	US 61087 77 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
170	US 61065 73 A	<input checked="" type="checkbox"/>	Apparatus and method for tracing microprocessor instructions	717/128
171	US 61015 82 A	<input checked="" type="checkbox"/>	Dcbst with icbi mechanism	711/141
172	US 60918 96 A	<input checked="" type="checkbox"/>	Debugging optimized code using data change points	717/125
173	US 60885 25 A	<input checked="" type="checkbox"/>	Loop profiling by instrumentation	717/150
174	US 60853 33 A	<input checked="" type="checkbox"/>	Method and apparatus for synchronization of code in redundant controllers in a swappable environment	714/7
175	US 60818 86 A	<input checked="" type="checkbox"/>	Holding mechanism for changing operation modes in a pipelined computer	712/229
176	US 60759 37 A	<input checked="" type="checkbox"/>	Preprocessing of stored target routines for controlling emulation of incompatible instructions on a target processor and utilizing target processor feedback for controlling non-sequential incompatible instruction emulation	703/23
177	US 60732 17 A	<input checked="" type="checkbox"/>	Method for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
178	US 60552 11 A	<input checked="" type="checkbox"/>	Force page zero paging scheme for microcontrollers using data random access memory	365/238 .5
179	US 60527 71 A	<input checked="" type="checkbox"/>	Microprocessor with pipeline synchronization	712/34

	Document ID	U	Title	Current OR
180	US 60473 67 A	<input checked="" type="checkbox"/>	Microprocessor with improved out of order support	712/23
181	US 60471 25 A	<input checked="" type="checkbox"/>	Garbage collection system for improved use of memory by removal of reference conflicts	717/148
182	US 60444 53 A	<input checked="" type="checkbox"/>	User programmable circuit and method for data processing apparatus using a self-timed asynchronous control structure	712/201
183	US 60262 37 A	<input checked="" type="checkbox"/>	System and method for dynamic modification of class files	717/130
184	US 60237 58 A	<input checked="" type="checkbox"/>	Method and processor for changing program by replacing instruction stored in ROM with predetermined value to be interpreted as an instruction	712/220
185	US 60214 81 A	<input checked="" type="checkbox"/>	Effective-to-real address cache managing apparatus and method	711/207
186	US 60212 65 A	<input checked="" type="checkbox"/>	Interoperability with multiple instruction sets	712/209
187	US 60095 16 A	<input checked="" type="checkbox"/>	Pipelined microprocessor with efficient self-modifying code detection and handling	712/244
188	US 60028 81 A	<input checked="" type="checkbox"/>	Coprocessor data access control	712/34
189	US 60000 14 A	<input checked="" type="checkbox"/>	Software-managed programmable congruence class caching mechanism	711/128
190	US 59997 32 A	<input checked="" type="checkbox"/>	Techniques for reducing the cost of dynamic class initialization checks in compiled code	717/148
191	US 59960 71 A	<input checked="" type="checkbox"/>	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
192	US 59951 02 A	<input checked="" type="checkbox"/>	Server system and method for modifying a cursor image	345/856
193	US 59745 38 A	<input checked="" type="checkbox"/>	Method and apparatus for annotating operands in a computer system with source instruction identifiers	712/218
194	US 59742 40 A	<input checked="" type="checkbox"/>	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
195	US 59681 74 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a 32-bit operating system which supports 16-bit code	713/2
196	US 59681 35 A	<input checked="" type="checkbox"/>	Processing instructions up to load instruction after executing sync flag monitor instruction during plural processor shared memory store/load access synchronization	709/400
197	US 59665 30 A	<input checked="" type="checkbox"/>	Structure and method for instruction boundary machine state restoration	712/244
198	US 59648 93 A	<input checked="" type="checkbox"/>	Data processing system for performing a trace function and method therefor	714/39
199	US 59637 41 A	<input checked="" type="checkbox"/>	Information processor which rewrites instructions in program to dynamically change program structure and method therefor	717/111
200	US 59637 40 A	<input type="checkbox"/>	System for monitoring computer system performance	717/130

	L #	Hits	Search Text	DBs
1	L2	3542	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code)).ab,ti.	USPAT; US-PGPUB
2	L4	14410	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address))	USPAT; US-PGPUB
3	L6	2604	execut\$3 near30 4	USPAT; US-PGPUB
4	L8	522	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut\$3	EPO; JPO; DERWENT; IBM TDB
5	L9	22638	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code)).ab,ti.	EPO; JPO; DERWENT; IBM TDB
6	L10	458	8 and 9	EPO; JPO; DERWENT; IBM TDB
7	L11	5	8 and patch\$3	EPO; JPO; DERWENT; IBM TDB
8	L12	2657	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut\$3	USPAT; US-PGPUB
9	L13	3	2 and 12 not 7	USPAT; US-PGPUB
10	L15	423	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; JPO; DERWENT; IBM TDB
11	L16	195	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; DERWENT; IBM TDB
12	L7	385	2 and 6	USPAT; US-PGPUB
13	L17	187	7 and @pd<19991006	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 54758 52 A	<input type="checkbox"/>	Microprocessor implementing single-step or sequential microcode execution while in test mode	714/34
2	US 53455 70 A	<input type="checkbox"/>	Microprogram control circuit	712/248
3	US 47076 61 A	<input type="checkbox"/>	Machine generation of machine-executable state-change instructions for magnetic resonance imaging	324/309

	Document ID	U	Title	Current OR
1	EP 13653 08 A2	<input type="checkbox"/>	Method and apparatus for minimizing differential power attacks on processors	
2	WO 20866 52 A1	<input checked="" type="checkbox"/>	PROCESSOR	
3	EP 11090 96 A2	<input checked="" type="checkbox"/>	Processor and method of controlling the same	
4	FR 27891 93 A1	<input checked="" type="checkbox"/>	Method for modifying behavior of computer under execution of functions in binary code by replacing first branching instruction by second branching instruction at first determined address	
5	EP 99778 7 A2	<input checked="" type="checkbox"/>	Image forming apparatus for managing copy sheets individually	
6	EP 88939 3 A2	<input checked="" type="checkbox"/>	Force page zero paging scheme for microcontrollers	
7	WO 98546 39 A1	<input checked="" type="checkbox"/>	PATCHING APPARATUS AND METHOD FOR UPGRADING MODEM SOFTWARE CODE	
8	WO 98374 67 A1	<input checked="" type="checkbox"/>	PERSONAL COMPUTER-INCORPORATED NUMERICAL CONTROL APPARATUS, AND IMAGE TRANSFER METHOD FOR PERSONAL COMPUTER-INCORPORATED NUMERICAL CONTROL APPARATUSES	
9	EP 78550 4 A2	<input checked="" type="checkbox"/>	Out of order execution of load instructions in a superscalar processor	
10	EP 73683 0 A1	<input checked="" type="checkbox"/>	Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor	
11	EP 69677 2 A2	<input checked="" type="checkbox"/>	Register file with multi-tasking support	
12	EP 59744 1 A1	<input checked="" type="checkbox"/>	Microprocessor having a bus-width change function.	
13	EP 43132 6 A2	<input checked="" type="checkbox"/>	Inter-processor interrupts in an n-element multi-processor.	
14	EP 32719 5 A2	<input checked="" type="checkbox"/>	Processor simulation.	
15	FR 25824 21 A1	<input checked="" type="checkbox"/>	Identity authentication apparatus	
16	EP 20262 8 A2	<input checked="" type="checkbox"/>	Instruction monitor used for a stored-program data processor.	
17	WO 86050 15 A1	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLER	
18	GB 20405 19 A	<input checked="" type="checkbox"/>	Improvements in or Relating to Data Processing Systems	
19	GB 20167 53 A	<input checked="" type="checkbox"/>	Data Processing System	
20	NN820 14018	<input checked="" type="checkbox"/>	Instruction Execution Conditioned on Operand Addresses. January 1982.	
21	NN710 22505	<input checked="" type="checkbox"/>	Re Enterable Programming. February 1971.	
22	US 20040 02516 5 A	<input checked="" type="checkbox"/>	Operating system functionality extending method for supporting new protocol, involves determining if functionality is to be modified to execute code stored by dynamic execution layer interface, to implement modified functionality	

	Document ID	U	Title	Current OR
23	US 66913 08 B	<input checked="" type="checkbox"/>	Hot patch circuit for changing micro code to be executed in processor, has cache system that selectively compares, for each address generated by program counter, generated address to addresses stored in cache system	
24	JP 20040 49433 A	<input checked="" type="checkbox"/>	Game machine e.g. pachinko machine controls display of special specific presentation display in scrolling game from series of continuous presentation display, based on determination result	
25	US 20040 01977 0 A	<input checked="" type="checkbox"/>	Optimization apparatus for computer, has generation unit which generates dummy instruction and controller that performs optimization by changing execution instruction order over dummy instruction	
26	CN 14472 44 A	<input checked="" type="checkbox"/>	Method designed in CPU for detecting buffer area overflow	
27	US 20030 20869 6 A	<input checked="" type="checkbox"/>	Computer system stores encoded password and configuration data in read only memory, which are modified by system management interrupt-based code executed by central processing unit	
28	US 66315 20 B	<input checked="" type="checkbox"/>	Execution code changing method of microcontroller, involves loading overlay code in second page of memory, asserting overlay flags for selected portions of default code and substituting overlay code in those portions	
29	US 66257 01 B	<input checked="" type="checkbox"/>	Data processing method in multiprocessor data processing system, involves modifying contents of memory corresponding to selected address, by executing stored conditional instruction	
30	US 20030 16742 3 A	<input checked="" type="checkbox"/>	Program product for testing consistency of machine code and source files, has instructions executed to produce source file attribute record including file location information, file modified date, during compilation of file source code	
31	US 20030 14531 4 A	<input checked="" type="checkbox"/>	Program optimizing method in network computer, involves modifying program to be executed to include optimized sequence of instructions comprising prefetch instructions, when cache misses occurs	
32	JP 20031 98362 A	<input checked="" type="checkbox"/>	Processing system for general-purpose computer, has shift register with field programmable gate array data memories storing respective modules of large scale program, of which appropriate one is selected and executed	
33	US 20030 08422 9 A	<input checked="" type="checkbox"/>	Read only memory program modification method for embedded systems, involves modifying code segments of read only memory by executing replacement code segment of random access memory	
34	US 65499 89 B	<input checked="" type="checkbox"/>	Cache coherency management method in multiprocessor data processing system, involves indicating reservation continuing and releasing states of selected address, during modification of contents of associated cache	
35	US 20030 06901 6 A	<input checked="" type="checkbox"/>	Recorded medium stores instruction for executing return of acknowledgement, on reception of address change machine of mobile host over secured control channel	
36	US 20030 06747 3 A	<input checked="" type="checkbox"/>	Predefined code set execution method for programmable vertex shader, involves executing specified substitute instructions using intermediate result obtained by executing another instruction using not more than n input operands	
37	US 65500 58 B	<input checked="" type="checkbox"/>	Computer executable code generation method for multitask program stack management, involves inserting stack clearing code in return operations for clearing stack memory to prevent usage of residual data in stack	
38	JP 20030 68019 A	<input checked="" type="checkbox"/>	Optical disk apparatus includes comparator which compares key code for overwriting stored in buffer memory and key code stored in non-volatile memory	
39	US 20030 04666 2 A	<input checked="" type="checkbox"/>	Data reproduction apparatus used in e.g. electronic publishing, has script analysis and execution unit that controls data reproduction according to specified reproduction instruction	

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40	US 20030 02875 7 A	<input checked="" type="checkbox"/>	Instructions modifying method for uniprocessor system, involves overwriting memory location with value representing patch class instruction concurrent with execution of another. value representing patch class instruction	
41	US 20030 00521 2 A	<input checked="" type="checkbox"/>	Stored program modification method for use in PC, involves invoking address match routine to execute portion of correction code during program execution	
42	JP 20030 67152 A	<input checked="" type="checkbox"/>	Image processor e.g. printer, facsimile, scanner, copier, has rewriting instruction unit that provides instructions to firmware rewriting unit to overwrite firmware stored in memory	
43	FR 28283 05 A	<input checked="" type="checkbox"/>	Protection of software against unauthorized use, reproduction or alteration, e.g. for protection of chip card software or software protected by a material key associated with a USB port using a principle of a verification variable	
44	GB 23790 57 A	<input checked="" type="checkbox"/>	Memory operations testing method for computer program development detects accesses to unmapped region of two-region virtual memory associated with physical memory	
45	EP 12800 56 A	<input checked="" type="checkbox"/>	Linking object code modules to form executable program by deriving call frame information instructions from call frame information macros	
46	US 20020 19906 7 A	<input checked="" type="checkbox"/>	Locked-memory instruction execution method in multi-threaded processor system, involves merging modified version of load data value and stored load data value, when un-snooped condition of cacheline is determined	
47	US 20020 17413 6 A	<input checked="" type="checkbox"/>	Database management system optimization method involves updating summary table in solid state disk, corresponding to manipulations of data in reconstructed tables	
48	WO 20028 9146 A	<input checked="" type="checkbox"/>	Testing an embedded memory array, an instruction or a series of consecutively executed instructions are repeated with modifications to the instruction fields of each command, specific instructions have an active repeat control field	
49	WO 20028 6652 A	<input checked="" type="checkbox"/>	Processor has instruction decoder that issues an instruction to a data path block	
50	US 20020 15698 1 A	<input checked="" type="checkbox"/>	System management RAM implementation method in computer systems, involves caching extended memory by changing cache settings using write-back and uncaching SMRAM upon execution of resume instruction	
51	WO 20027 7822 A	<input checked="" type="checkbox"/>	Monitoring run time execution of software code by inserting routine into buffer with data or cache disabling instruction	
52	US 20020 12082 9 A	<input checked="" type="checkbox"/>	Data processor for cellular phone, has buffer controller circuit that validates flag of buffer, when instruction is prefetched into that buffer	
53	US 20020 11214 9 A	<input checked="" type="checkbox"/>	Program execution method in data processing system, involves selecting jump address by comparing output of program counter with preset value	
54	US 20020 09193 4 A	<input checked="" type="checkbox"/>	Encrypted viral code decryption detection method for computer virus detection, involves detecting modification to flagged memory area during emulation of specific instruction in completely executable code	
55	US 20020 08781 0 A	<input checked="" type="checkbox"/>	Locked-memory instruction execution method in microprocessor, involves merging modified load data value with stored load data value after determination of unsnooped condition of cacheline	
56	US 20020 07332 3 A	<input checked="" type="checkbox"/>	Virus detection method in computer system involves monitoring emulation of computer executable code and modification of memory state to detect attempt by emulated code to access restricted computer system resources	
57	US 20020 04630 5 A	<input checked="" type="checkbox"/>	Foreign binary code translating system for computer, stores page tables representing memory allocation in response to changes generated by executing binary translated codes	

	Document ID	U	Title	Current OR
58	TW 480396 A	<input checked="" type="checkbox"/>	Method capable of simultaneously storing program code and data in flash memory - capable of greatly improving data modification efficiency of flash memory	
59	US 6356918 B	<input checked="" type="checkbox"/>	Register array management method in data processing system, involves storing instruction execution result in address acquired from rename table, and moving next address from completion table to rename table	
60	US 6349366 B	<input checked="" type="checkbox"/>	Memory management system for multiprocessor shared memory system, outputs probe command through system port to target processor, so that state of data block of processor is changed in accordance with probe command	
61	US 6336212 B	<input checked="" type="checkbox"/>	Software application for testing addressing modes in microprocessor, modifies test code which executes several instructions, to test incremented addressing mode and initializes data used by addressing modes	
62	US 6317870 B	<input checked="" type="checkbox"/>	Inter-module procedure call optimization for computer program, involves modifying call instruction to directly call unresolved module at determined location, once unresolved module is called during program execution	
63	US 20010032327 A	<input checked="" type="checkbox"/>	Memory processing method for microcontroller, involves selecting object code having matching skipped-code-address range based on detection result of defective addresses in memory and loading into memory for execution	
64	WO 200175605 A	<input checked="" type="checkbox"/>	Debugging an executing service on pipelined CPU architecture, involves setting break point including altering instruction within execution service and invalidating page cache of the execution service	
65	CN 1308337 A	<input checked="" type="checkbox"/>	Simultaneous program code and data storing method in flash memory	
66	US 20010010072 A	<input checked="" type="checkbox"/>	Instruction translator for non-native instructions for processor, has selector for selectively outputting instruction output by translator and corresponding instruction held in instruction cache	
67	CN 1303043 A	<input checked="" type="checkbox"/>	Basic cache block microprocessor changes execution of instructions, based on instruction history information showing exception event relating to instruction group	
68	EP 1111510 A	<input checked="" type="checkbox"/>	Program modification device for computer system, has instruction switch which replaces program data and addresses, in order to make execution unit read modification target program data instead of source address data	
69	JP 2001166935 A	<input checked="" type="checkbox"/>	Branch instruction address estimation procedure for processor, involves executing branch instructions sequentially, by judging validity of the assigned addresses	
70	US 20010004757 A	<input checked="" type="checkbox"/>	Processor that performs a load operation prior to a store operation while avoiding ambiguous memory reference, and achieves high-speed operations using history control unit for controlling out-of-order processes	
71	US 6243807 B	<input checked="" type="checkbox"/>	Computer architecture performance optimization method involves retrieving function information as single block from external memory into cache memory when executing loop routine	
72	US 6243789 B	<input checked="" type="checkbox"/>	Program code execution in dynamic random access memory, involves resuming program execution, after copying and remapping page of flash EEPROM, attempted to be modified by program, to RAM	
73	US 6237088 B	<input checked="" type="checkbox"/>	In-flight instruction tracking apparatus in pipeline of microprocessor, compares line address associated with fetched instruction in pipeline, with address of stored instruction, to detect SMC conflict	
74	JP 2001092663 A	<input checked="" type="checkbox"/>	Data processor of sto add program type digital computer, processes memory access instruction by dynamically changing the execution time and calculation instruction according to execution time determined statically	
75	SE 200000447 A	<input checked="" type="checkbox"/>	Encryption device, used to encrypt information packets comprising non encrypted text data block and block header	

	Document ID	U	Title	Current OR
76	WO 20011 4965 A	<input checked="" type="checkbox"/>	Data processor transfers control from subprogram stored in auxiliary memory to various instructions in memory temporarily after suspending data change and before change is completed	
77	KR 20010 03246 A	<input checked="" type="checkbox"/>	Method for managing feature codes using shared memory in home location register	
78	WO 20006 8784 A	<input checked="" type="checkbox"/>	Data processing device for executing load instructions, modifies data handling, and primary and secondary memory access instruction programs command to compensate out of order execution of memory access instruction	
79	US 61287 27 A	<input checked="" type="checkbox"/>	Addressing mode testing of microprocessor, involves using self modifying code so that test instruction executed to test one addressing mode is modified to use for next testing	
80	JP 20002 42484 A	<input checked="" type="checkbox"/>	Control program modification method for computer system, involves dividing execution code and data code during first stage loading on main memory unit	
81	US 61087 97 A	<input checked="" type="checkbox"/>	Automatic program code modification method for memory chips, involves bypassing dummy codes by inserting jump instruction to obtain modified program code	
82	JP 20002 22242 A	<input checked="" type="checkbox"/>	Compilation of Java program in network computing, involves storing address of execution code which changes stack pointer and information about size of stack frame after change, in memory	
83	FR 27891 93 A	<input checked="" type="checkbox"/>	Method for modifying behavior of computer under execution of functions in binary code by replacing first branching instruction by second branching instruction at first determined address	
84	US 20020 02934 6 A	<input checked="" type="checkbox"/>	Conditional jump operation masking in cryptographic processor, involves executing different number of instructions for each conditional jump, for each evaluation of distinguishing value against reference value	
85	US 60732 17 A	<input checked="" type="checkbox"/>	Instruction update snooping method for superscalar microprocessors, involves deleting address from buffer for updating instructions, if inequality occurs in address stored in buffer and update address	
86	US 60556 31 A	<input checked="" type="checkbox"/>	Booting method for personal digital assistant	
87	US 60498 66 A	<input checked="" type="checkbox"/>	User mode cache synchronization for MIPS architecture computer system, involves changing certain entries of instruction cache in specific address range as invalid during cache synchronization instruction execution	
88	JP 20000 47863 A	<input checked="" type="checkbox"/>	Information processor for video game apparatus, generates jump instruction to the address where the modified part of program is stored in external memory	
89	US 59912 00 A	<input checked="" type="checkbox"/>	Erasing control circuit for batch erasable type EEPROM, flash EPROM in microcomputer system	
90	US 59499 73 A	<input checked="" type="checkbox"/>	Stack override prevention method of computer operating system	
91	US 59408 59 A	<input checked="" type="checkbox"/>	Floating point and packed data instructions execution method for multimedia applications	
92	JP 11143 597 A	<input checked="" type="checkbox"/>	Microprocessor - has low power consumption decision circuit that outputs low power consumption mode signal which changes microprocessor or power save mode circuit into low power consumption condition	
93	US 59058 81 A	<input checked="" type="checkbox"/>	Delayed state write apparatus for memory in pipelined instruction processor of data processing system	
94	US 58976 65 A	<input checked="" type="checkbox"/>	Register addressing for register architecture used for microprocessor, microcontroller	

	Document ID	U	Title	Current OR
95	RD 41911 9 A	<input checked="" type="checkbox"/>	Suspending threads at safe points - involves suspending thread until handler is called for thread execution	
96	JP 11065 843 A	<input checked="" type="checkbox"/>	Microprocessor for pipeline processing - changes order of execution according to dependence of prefetched instruction with instruction stored in memory	
97	US 58812 76 A	<input checked="" type="checkbox"/>	Manipulation of protected pages to reduce conditional statements usage in coded program	
98	US 58812 72 A	<input checked="" type="checkbox"/>	Parallel processors synchronization system for image and graphics processing system	
99	JP 11039 150 A	<input checked="" type="checkbox"/>	Micro controller - has CPU which executes control program stored in flash memory during change of mode based on input specific instruction code which does not change program counter value	
100	US 60444 35 A	<input checked="" type="checkbox"/>	Machine readable storage device embodying instructions executable by memory controller of memory management subsystem - tests if modifications made to lists of tape drives available to serve requests in modified request queue allow n different drives to be assigned to n requests	
101	JP 11015 793 A	<input checked="" type="checkbox"/>	Simultaneous instruction execution method in computer system - involves setting resources order wise so as to prevent its modification during instruction execution by adjacent processors, based on usability or non-usability of resources lock status	
102	US 58623 85 A	<input checked="" type="checkbox"/>	Compiling method for program execution in computer - involves compiling reordered intermediate code into object code and is ultimately executed which generates less cache conflicts than that of when initial intermediate code is compiled and executed	
103	JP 10340 210 A	<input checked="" type="checkbox"/>	Task debug apparatus for operating system - interrupts process of T system for corresponding task and address when output signals of address event detector output controller and instruction execution event detector are in active condition	
104	WO 98572 55 A	<input checked="" type="checkbox"/>	Modification of code sequences. - using active orientation instructions to obtain time delay after which rerouting to new address takes place.	
105	US 58386 94 A	<input checked="" type="checkbox"/>	Dual source data distribution system for integrated circuit tester - has distributed memories to store test vectors and central control to instruct execution or altering of test vectors	
106	US 58359 49 A	<input checked="" type="checkbox"/>	Pipelined microprocessor for computer system - flushes execution pipeline in response to instruction written to address within primary instruction cache	
107	EP 87112 5 A	<input checked="" type="checkbox"/>	Logic module e.g. for implementing system changes on PC architecture computers - has transceiver module and memory module containing storage elements and executable code stored as pages with logic card having page register module in communication with transceiver and memory	
108	US 58121 33 A	<input checked="" type="checkbox"/>	Industrial controller for mixing tank - has address monitor that alters display of graphical element when electronic memory is accessed by address corresponding to identified graphic element	
109	US 58025 73 A	<input checked="" type="checkbox"/>	Data processing system execution simulation method - involves initializing target locations and storing them in queues corresponding to store instruction and load instruction	
110	JP 10105 537 A	<input checked="" type="checkbox"/>	Simulation system with facility for modifying setting parameters during simulation program execution - includes shared memory in which instructions input by input-output interface unit are stored and later read out to execute simulation program corresponding to changed parameter	
111	RD 40809 2 A	<input checked="" type="checkbox"/>	Propagating memory cache hits and misses to software - using control bit in processor to modify manner in which memory load instructions are executed	

	Document ID	U	Title	Current OR
112	US 57297 57 A	<input checked="" type="checkbox"/>	Super computer system architecture using status memory to alter program - has instruction sequencing under program control computer, with individual instructions assigned for execution to individual instruction computer, and modifiable micro-tasks to execute instruction between successive or during single cycle	
113	US 57175 87 A	<input checked="" type="checkbox"/>	Method of recording non-effective instruction in data processing system - involves re-coding selected instruction into specified instruction format prior to further processing of selected instruction	
114	JP 10020 907 A	<input checked="" type="checkbox"/>	Sequence control method for designing and modification of sequence circuit - involves executing instruction of lower order module using input-output address of control object obtained by converting command from higher order module with reference to address parameter table	
115	EP 81051 7 A	<input checked="" type="checkbox"/>	Hardware mechanism for avoiding thrashing caused by data or instruction prefetched to cache memory - has prefetch instruction buffer which is communication with prefetch execution unit for storing augmented prefetch instructions for retrieval at execution of prefetch instruction	
116	JP 09311 786 A	<input checked="" type="checkbox"/>	Data processor e.g. microprocessor, microcomputer - executes instruction of second instruction format which is altered from instruction of first instruction format stored in instruction memory	
117	US 56550 96 A	<input checked="" type="checkbox"/>	Pipelined program execution method with exception handling - involves dynamically determining instruction execution point when instructions are executed in non-sequential program order knowing when previous source location writes and reads and writes of destination locations will be completed	
118	US 56405 60 A	<input checked="" type="checkbox"/>	Method of modifying multimedia recorded on non-volatile medium e.g CD-ROM - involves transferring machine instructions that implement filter to memory of computer that is to execute multimedia work for execution by computer	
119	TW 30244 5 A	<input checked="" type="checkbox"/>	Load queue for bypassing in a load/store unit of a superscalar processor - includes real page number buffer for storing real page numbers for instruction entries in queue and real page number comparator for comparing executing load instructions with queued load instruction entries	
120	EP 74906 3 A	<input checked="" type="checkbox"/>	Code execution control method for suspend/resume operation in computer - using multiple suspend files to save multiple system states, and multiple operating systems requiring multiple swap files	
121	EP 74024 8 A	<input checked="" type="checkbox"/>	Responding to trapping conditions in pipelined computer - involves distinguishing between hardware traps and software traps, forwarding software trapping instruction to execute stage and changing fetch address	
122	JP 08106 383 A	<input checked="" type="checkbox"/>	Operation processor e.g. microprocessor, digital signal processor - provided with control signal output by first and second decoder for RISC and CISC after scanning command setting from memory based on execution of clock and performs operation processing after receiving data directly from memory	
123	JP 08030 307 A	<input checked="" type="checkbox"/>	Controlled system processes order controller for vegetable growing hot house temp. - has value replaced by back-and-front process and starting order and changed automatically with changed setting time displayed on operation display	
124	GB 22903 95 A	<input checked="" type="checkbox"/>	Data processing appts with multiple program instruction function - has controller that controls processor core to execute program instruction word in response to predetermine indicator bit of program counter register	
125	US 54758 52 A	<input checked="" type="checkbox"/>	Pipeline microprocessor - includes test mode for executing whole microprogram routine and one microinstruction of arbitrary address in micro ROM to diagnose internal functions and unit for changing sequence field and executes between two continuous instruction	
126	US 54695 50 A	<input checked="" type="checkbox"/>	Reversible computer instruction execution unit - has CPU with microinstruction memory programmed to support forward and reverse execution instructions with restoration of data values overwritten by forward instruction if needed	

	Document ID	U	Title	Current OR
127	US 55817 20 A	<input checked="" type="checkbox"/>	Information updating circuit for microcode instruction without interrupting program execution - periodically accesses instruction for execution from memory and selectively alters program information within microcode instruction stored in memory	
128	JP 07264 471 A	<input checked="" type="checkbox"/>	Special effect device with switch maintaining execution speed of key frame - has rotary control changing execution speed of key frame stored in memory controlled by entered instructions NoAbstract	
129	GB 22873 34 A	<input checked="" type="checkbox"/>	Maintaining memory consistency in pipeline, non-blocking caching bus request queue - includes external bus request queue for ensuring that request to same address are issued and serviced on bus according to set memory ordering scheme	
130	EP 73733 4 B	<input checked="" type="checkbox"/>	Pipelined micro-instruction system with branch prediction and speculative changing - uses multi-stage pipelining and branch prediction to enable speculative changes of state during execution of predicted instruction before determining prediction accuracy	
131	US 54106 85 A	<input checked="" type="checkbox"/>	Non-intrusive method for recovering state of computer system - using memory having two matched levels, with checkpoint instructions causing target processor to cue checkpoint processor to initiate checkpoint process	
132	EP 64091 6 A	<input checked="" type="checkbox"/>	Microcomputer with instruction executing unit and program memory - has executing unit and program memory with counter successively indicating addresses to output contents through interface with comparator giving selection signal if true	
133	US 53922 07 A	<input checked="" type="checkbox"/>	Method of programming motion controller for control of industrial servo-motors - requires initially selecting graphical icons, each icon representing sequential step in control of motor, and displaying on electronic display	
134	US 53773 36 A	<input checked="" type="checkbox"/>	Pre-fetching data for load instruction before transfer to execution unit - processing data fetch in load instructions in load unit which predicts address for data fetch such that fetch can occur earlier than in typical load processing	
135	US 53455 67 A	<input checked="" type="checkbox"/>	Modifying program status word system mask, access key, and address space code system with overlap enabled - has register device coupled to execution unit and to queue device for storing standardised program status word, which is program status word in subsystem	
136	JP 06125 275 A	<input checked="" type="checkbox"/>	Signal processing device with A=D converter for e.g. magnetic recording/reproducing device - has circuits for analog input, reference signal detection and thermometer signal generation	
137	EP 61455 0 B	<input checked="" type="checkbox"/>	Self-programming microcontroller with stored instruction to command program - uses instruction to program the program memory and autoincrementing pointer and on-chip ROM used to store program	
138	EP 53982 7 A	<input checked="" type="checkbox"/>	Dynamic instruction modifying controller for computer - includes execution device and memory having control program which communicates to execution unit via conductor	
139	EP 56571 2 B	<input checked="" type="checkbox"/>	Network structure for parallel processing computer programs - uses large number of highly efficient virtual processors derived from large memory banks in the core of the network	
140	US 52029 64 A	<input checked="" type="checkbox"/>	Interface controller including messaging scanner accessing state action table - has peripheral unit state changes detected in scanning mode to access state action table for assembling program addresses and microcodes	
141	EP 52566 6 A	<input checked="" type="checkbox"/>	Information-processing microcomputer with branch target instruction buffer - transfers selected branch target instruction immediately to execution unit without waste of bus cycle during fetch	
142	EP 50706 6 A	<input checked="" type="checkbox"/>	Ownership interlock for caches in data processing systems - prevents any processor ownership change to occur for cache data unit until all outstanding stores have been made	
143	US 51426 30 A	<input checked="" type="checkbox"/>	Instruction precontrol system for data processing unit - calculates branch destination address based on address mode bit in operand before executing instruction with changes address mode and branching	
144	EP 49748 5 A	<input checked="" type="checkbox"/>	Data processing system with two operand instruction implementation - does not write result produced by operation to memory if destination value is unchanged	

	Document ID	U	Title	Current OR
145	US 51135 14 A	<input checked="" type="checkbox"/>	Multiple-level multiprocessor cache memory organisation method - defining status of each cache with tag bit and updating tag bits with instruction execution	
146	EP 45326 8 A	<input checked="" type="checkbox"/>	Microprocessor for inserting bus cycle to output internal information - has bus controller coupled to other processors to enable insertion of bus cycle in accordance with bus cycle request signal	
147	EP 45046 2 A	<input checked="" type="checkbox"/>	Method for updating stored program information in ROM - using normal mode to down load information from ROM and changing to programming mode reprogramming memory	
148	EP 44547 9 A	<input checked="" type="checkbox"/>	Peripheral sub-system for bulk memory - uses automatic peripheral controller to off load central processor in handling multiple bulk storage devices	
149	US 52261 30 A	<input checked="" type="checkbox"/>	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
150	EP 43132 6 A	<input checked="" type="checkbox"/>	Inter-processor for MP computer system - generates interrupt request if zero is not detected on all low data being written to memory	
151	EP 41917 4 A	<input checked="" type="checkbox"/>	Improved data processor with microprogram control - includes microinstruction execution unit which operates its pipeline process and resumes operation by using corrected parameters	
152	EP 40843 1 A	<input checked="" type="checkbox"/>	Storage and restoration of modifiable programme executed by processor - uses read only memory to store executable code for program units and reprogrammable memory to store program modifications	
153	EP 40176 3 A	<input checked="" type="checkbox"/>	Control timing signal generator - for mobile telephone performed by both absolute and relative time, and suitable for equipment control requiring numerous timing signals	
154	DE 40123 47 A	<input checked="" type="checkbox"/>	VCR remote controller memory addressing appts. - modifies RAM data by storing group initial addresses to form executable instructions	
155	EP 38852 6 A	<input checked="" type="checkbox"/>	Programmable channel error inspection method and appts. - with means to time recovery of inspected errors is used for testing data processing system	
156	EP 38085 8 A	<input checked="" type="checkbox"/>	Error handling method for pipelined computer system - distinguishes between errors that prevent instructions completing and those that do affect instructions	
157	EP 36518 8 A	<input checked="" type="checkbox"/>	Programmable computer executing contiguous instructions in sequence - reduces delays in response to branch instructions using separate updated condition codes determined from previous instructions	
158	EP 36356 7 A	<input checked="" type="checkbox"/>	Computer system with interrupt controlled clock speed - has machine language program which changes speed of oscillator clock when interrupt is generated	
159	US 49145 84 A	<input checked="" type="checkbox"/>	Intermediate code memory for buffering code segments - is located between main memory and processor to prefetch code and supply in-line instruction stream to processor	
160	EP 35923 3 A	<input checked="" type="checkbox"/>	Computer system and method for changing operation speed of system bus - generates frequency change instruction in response to execution of program, and has system bus operation clock with variable frequency	
161	EP 32719 5 A	<input checked="" type="checkbox"/>	Application program processor simulating data processor - reduces number of translated instructions needed to simulate flow of control of instructions	
162	EP 31913 2 A	<input checked="" type="checkbox"/>	Data processing system for handling interrupts - allows interrupts to be handled while providing concurrent execution of instructions	
163	EP 31527 5 A	<input checked="" type="checkbox"/>	Flexible ASIC microcomputer - has random access memory user defined dedicated functions and programmable read only memory	
164	AU 88187 90 A	<input checked="" type="checkbox"/>	Measurement of instruction execution for computer program - has selected instruction replaced with measurement instruction with indication of selected execution then restores and executes original	

	Docum ent ID	U	Title	Current OR
165	EP 29789 5 A	<input checked="" type="checkbox"/>	Main memory updating in multiprocessor system - provides read, mask, add, quad word, interlocked instruction to synchronise loading or augmenting of data elements in main memory	
166	EP 29789 0 A	<input checked="" type="checkbox"/>	Data processor fault condition response system - generates boolean valve indicating operation validity for storage at predetermined register position to initiate fault condition signal	
167	EP 27517 0 A	<input checked="" type="checkbox"/>	Instruction decoder for variable byte processor - enables processing of different operands stored at different addresses by repeating operation, addresses being specified sequentially	
168	EP 27012 5 A	<input checked="" type="checkbox"/>	High speed pipeline control system for calculator - divides instruction into several states and processes it so respective stages are operated in parallel to each other	
169	EP 26514 8 A	<input checked="" type="checkbox"/>	Operating microprocessor controlled device e.g. bar code reader - by directly manipulating memory locations in microprocessor hardware by scanning bar code tags selected from menu	
170	EP 25518 6 A	<input checked="" type="checkbox"/>	Parallel processing system for functional languages - has processors executing side effecting instructions modifying memory contents and functional instructions for locations in main memory	
171	EP 23908 1 A	<input checked="" type="checkbox"/>	Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed	
172	EP 23003 8 A	<input checked="" type="checkbox"/>	Data processor address generation system - has correction number generator to modify contents of register in instruction execution unit according to instruction code address field	
173	EP 22824 2 A	<input checked="" type="checkbox"/>	Non-intrusive microprocessor performance monitoring system - measures time spent at various parts of address space, in code execution and data accessing without altering real-time functions	
174	US 46758 10 A	<input checked="" type="checkbox"/>	Digital data processing system with organised memory system - uses object-based addressing having operand data identified by names accessed by name tables	
175	EP 20766 6 A	<input checked="" type="checkbox"/>	Moving string of bytes instruction in reduced instruction set computer - using compiler to generate optimised sequences instead of hardware to perform operations and pre-compute operands	
176	EP 18920 2 A	<input checked="" type="checkbox"/>	Microprogram control system - restores original micro instruction and assigned address by combining modified micro instructions and assigned addresses	
177	DE 35855 17 G	<input checked="" type="checkbox"/>	Microprocessor with variable memory capacity - uses bus changeover circuit which allows control of effective bit-width of data bus	
178	EP 17028 4 A	<input checked="" type="checkbox"/>	Microcomputer processing data stored in different register banks - executes single instruction using logic gates and selector circuits to effect data transfers among banks	
179	SU 11749 30 A	<input checked="" type="checkbox"/>	Diagnostic and control unit - has control switches taken across address register to memory at inputs of logic conditions switch and comparator	
180	WO 85031 50 A	<input checked="" type="checkbox"/>	Data processing system with memory hierarchy - has ROM for storing program to be executed, changeable memory for storing instructions to change program, and RAM for revised program	
181	US 44941 88 A	<input checked="" type="checkbox"/>	Multiprocessor system operating method - dividing system into concurrently executable units and checking whether ready state process is present for each unit	
182	RD 24904 3 A	<input checked="" type="checkbox"/>	Execute instruction to no-operation changing using linkage editor - having evaluated address constant added to execute instruction when NOP is required	
183	DE 34152 09 A	<input checked="" type="checkbox"/>	Data processor software security - address portion of instruction is modified when fetched from memory and restored before execution	
184	US 44344 64 A	<input checked="" type="checkbox"/>	Memory protection system for data processing system - effects alteration of protection information without intervention of control program when erroneous access is accepted	

	Document ID	U	Title	Current OR
185	EP 97234 A	<input checked="" type="checkbox"/>	Computer restarting system following normal or abnormal termination - maintains completion and operational states respectively of two structures w.r.t. subset of resource managers	
186	DE 32026 11 A	<input checked="" type="checkbox"/>	Computer processor simulation system - uses replacement of major part of processors control logic by variable memory controlled via programmable register to deliver control signal	
187	EP 66376 A	<input checked="" type="checkbox"/>	Data processing system with instruction buffer - pre-transfers instructions from main storage to buffer which is invalidated only when changed content is executed as instruction	
188	EP 59018 A	<input checked="" type="checkbox"/>	Multi-programmed data processing system with dynamic task assignment - requiring no centralised interrogation of all data processing devices	
189	US 42875 61 A	<input checked="" type="checkbox"/>	Address formulation interlock mechanism for processing system - uses two register identifying fields each having pre-decoded instruction entered into instruction queue	
190	US 41842 01 A	<input checked="" type="checkbox"/>	Integrating processor preventing data dissemination - executes instructions from internal memory which cannot be accessed by input-output processor	
191	DE 28170 73 A	<input checked="" type="checkbox"/>	Address processing for stored microinstructions of data processor - using address field modifier enabling prepared, direct and mixed linking modes	
192	US 40952 78 A	<input checked="" type="checkbox"/>	Instruction altering system for program control system - has multiplexer switched by coincidence output of comparator circuit	
193	US 39407 45 A	<input checked="" type="checkbox"/>	Computer with multiple hardware circuits - for processing at different priorities switched by priority change microinstruction	
194	FR 22608 29 A	<input checked="" type="checkbox"/>	Data processing method - has microprogrammes transferring and correcting memories and registers	
195	US 38919 72 A	<input type="checkbox"/>	Synchronous sequential controller for logic outputs - has medium scale integrated ccts. and logic gates connected together	

	L #	Hits	Search Text	DBs
1	L2	3542	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code)).ab,ti.	USPAT; US-PPGPUB
2	L4	14410	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address))	USPAT; US-PPGPUB
3	L6	2604	execut\$3 near30 4	USPAT; US-PPGPUB
4	L8	522	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut\$3	EPO; JPO; DERWENT; IBM_TDB
5	L9	22638	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 (instruction code)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
6	L10	458	8 and 9	EPO; JPO; DERWENT; IBM_TDB
7	L11	5	8 and patch\$3	EPO; JPO; DERWENT; IBM_TDB
8	L12	2657	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut\$3	USPAT; US-PPGPUB
9	L13	3	2 and 12 not 7	USPAT; US-PPGPUB
10	L15	423	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; JPO; DERWENT; IBM_TDB
11	L16	195	((chang\$3 alter\$3 modif\$6 overwrit\$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut\$3	EPO; DERWENT; IBM_TDB
12	L7	385	2 and 6	USPAT; US-PPGPUB
13	L17	187	7 and @pd<19991006	USPAT; US-PPGPUB

	Document ID	U	Title	Current OR
1	US 20040 01568 0 A1	<input type="checkbox"/>	Data processor for modifying and executing operation of instruction code	712/226
2	US 20030 17731 5 A1	<input checked="" type="checkbox"/>	Prefetch with intent to store mechanism	711/137
3	US 20030 16366 7 A1	<input checked="" type="checkbox"/>	Vector processing system	712/7
4	US 20030 15446 5 A1	<input checked="" type="checkbox"/>	Method and system for verifying modules destined for generating circuits	717/137
5	US 20030 13584 8 A1	<input checked="" type="checkbox"/>	Use of multiple procedure entry and/or exit points to improve instruction scheduling	717/158
6	US 20030 12641 4 A1	<input checked="" type="checkbox"/>	Processing partial register writes in an out-of order processor	712/225
7	US 20030 12088 0 A1	<input checked="" type="checkbox"/>	System having read-modify-write unit	711/155
8	US 20020 13870 2 A1	<input checked="" type="checkbox"/>	Using non-executable memory as executable memory	711/154
9	US 20020 08335 5 A1	<input checked="" type="checkbox"/>	Method and apparatus for dynamic power control of a low power processor	713/322
10	US 20010 04491 3 A1	<input checked="" type="checkbox"/>	Multiprocessor application interface requiring no utilization of a multiprocessor operating system	714/33
11	US 66810 58 B1	<input checked="" type="checkbox"/>	Method and apparatus for estimating feature values in a region of a sequence of images	382/294
12	US 66683 15 B1	<input checked="" type="checkbox"/>	Methods and apparatus for exchanging the contents of registers	712/219
13	US 66657 08 B1	<input checked="" type="checkbox"/>	Coarse grained determination of data dependence between parallel executed jobs in an information processing system	709/215
14	US 66403 15 B1	<input checked="" type="checkbox"/>	Method and apparatus for enhancing instruction level parallelism	714/17
15	US 65500 00 B1	<input checked="" type="checkbox"/>	Processor to execute in parallel plurality of instructions using plurality of functional units, and instruction allocation controller	712/215
16	US 65428 91 B1	<input checked="" type="checkbox"/>	Safe strength reduction for Java synchronized procedures	707/8
17	US 65395 00 B1	<input checked="" type="checkbox"/>	System and method for tracing	714/45
18	US 65229 58 B1	<input checked="" type="checkbox"/>	Logic method and apparatus for textually displaying an original flight plan and a modified flight plan simultaneously	701/3
19	US 65197 07 B2	<input checked="" type="checkbox"/>	Method and apparatus for dynamic power control of a low power processor	713/322

	Document ID	U	Title	Current OR
20	US 64250 86 B1	<input checked="" type="checkbox"/>	Method and apparatus for dynamic power control of a low power processor	713/322
21	US 63453 51 B1	<input checked="" type="checkbox"/>	Maintenance of speculative state of parallel executed jobs in an information processing system	711/203
22	US 63322 06 B1	<input checked="" type="checkbox"/>	High-speed error correcting apparatus with efficient data transfer	714/755
23	US 63306 57 B1	<input checked="" type="checkbox"/>	Pairing of micro instructions in the instruction queue	712/23
24	US 63083 22 B1	<input checked="" type="checkbox"/>	Method and apparatus for reduction of indirect branch instruction overhead through use of target address hints	717/145
25	US 62861 32 B1	<input checked="" type="checkbox"/>	Debugging support apparatus, a parallel execution information generation device, a computer-readable recording medium storing a debugging support program, and a computer-readable recording medium storing a parallel execution information generation program	717/125
26	US 62694 40 B1	<input checked="" type="checkbox"/>	Accelerating vector processing using plural sequencers to process multiple loop iterations simultaneously	712/241
27	US 62497 93 B1	<input checked="" type="checkbox"/>	Mostly concurrent compaction in a garbage collection system	707/206
28	US 62233 35 B1	<input checked="" type="checkbox"/>	Platform independent double compare and swap operation	717/100
29	US 61784 92 B1	<input checked="" type="checkbox"/>	Data processor capable of executing two instructions having operand interference at high speed in parallel	712/23
30	US 61122 89 A	<input checked="" type="checkbox"/>	Data processor	712/23
31	US 60092 65 A	<input checked="" type="checkbox"/>	Program product for optimizing parallel processing of database queries	707/3
32	US 60063 16 A	<input checked="" type="checkbox"/>	Performing SIMD shift and arithmetic operation in non-SIMD architecture by operation on packed data of sub-operands and carry over-correction	712/22
33	US 59745 38 A	<input checked="" type="checkbox"/>	Method and apparatus for annotating operands in a computer system with source instruction identifiers	712/218
34	US 59742 40 A	<input checked="" type="checkbox"/>	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
35	US 59405 16 A	<input checked="" type="checkbox"/>	Data security method and system	713/159
36	US 59371 99 A	<input checked="" type="checkbox"/>	User programmable interrupt mask with timeout for enhanced resource locking efficiency	710/262
37	US 59334 97 A	<input checked="" type="checkbox"/>	Apparatus and method for controlling access to software	705/59
38	US 59308 07 A	<input checked="" type="checkbox"/>	Apparatus and method for fast filtering read and write barrier operations in garbage collection system	707/206
39	US 58753 42 A	<input checked="" type="checkbox"/>	User programmable interrupt mask with timeout	710/260
40	US 58753 37 A	<input checked="" type="checkbox"/>	Modifier for a program executing parallel processes that reduces wait time for access to a shared resource	717/151
41	US 58505 43 A	<input checked="" type="checkbox"/>	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238

	Docum ent ID	U	Title	Current OR
42	US 58322 72 A	<input checked="" type="checkbox"/>	Apparatus and method for parallel computation	717/149
43	US 58226 08 A	<input checked="" type="checkbox"/>	Associative parallel processing system	712/20
44	US 58157 23 A	<input checked="" type="checkbox"/>	Picket autonomy on a SIMD machine	712/20
45	US 58154 21 A	<input checked="" type="checkbox"/>	Method for transposing a two-dimensional array	708/520
46	US 58092 92 A	<input checked="" type="checkbox"/>	Floating point for simid array machine	712/222
47	US 58023 38 A	<input checked="" type="checkbox"/>	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
48	US 57574 32 A	<input checked="" type="checkbox"/>	Manipulating video and audio signals using a processor which supports SIMD instructions	348/384 .1
49	US 57130 12 A	<input checked="" type="checkbox"/>	Microprocessor	712/233
50	US 56917 24 A	<input checked="" type="checkbox"/>	Police traffic radar using FFT processing to find fastest target	342/104
51	US 56597 94 A	<input checked="" type="checkbox"/>	System architecture for improved network input/output processing	710/1
52	US 56528 52 A	<input checked="" type="checkbox"/>	Processor for discriminating between compressed and non-compressed program code, with prefetching, decoding and execution of compressed code in parallel with the decoding, with modified target branch addresses accommodated at run time	712/208
53	US 56340 47 A	<input checked="" type="checkbox"/>	Method for executing branch instructions by processing loop end conditions in a second processor	712/241
54	US 56280 24 A	<input checked="" type="checkbox"/>	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions	712/23
55	US 55700 93 A	<input checked="" type="checkbox"/>	Police traffic radar using absolute signal strength information to improve target signal processing accuracy	342/104
56	US 55658 71 A	<input checked="" type="checkbox"/>	Police traffic radar for allowing manual rejection of incorrect patrol speed display	342/176
57	US 55636 03 A	<input checked="" type="checkbox"/>	Police traffic radar using digital data transfer between antenna and counting unit	342/115
58	US 55282 45 A	<input checked="" type="checkbox"/>	Police traffic radar using double balanced mixer for even order harmonic suppression	342/104
59	US 55259 96 A	<input checked="" type="checkbox"/>	Police traffic radar for calculating and simultaneously displaying fastest target speed	342/104
60	US 55155 35 A	<input checked="" type="checkbox"/>	System and method for parallel variable optimization	717/149
61	US 55112 07 A	<input checked="" type="checkbox"/>	Program control circuit determining the designated number of times a sequence of instructions is repetitively executed to prevent further execution of a jump instruction	712/241
62	US 55048 43 A	<input checked="" type="checkbox"/>	Apparatus and method for processing a stream of image data in a printing system	358/1.1 6
63	US 54407 03 A	<input checked="" type="checkbox"/>	System and method for saving state information in a multi-execution unit processor when interruptable instructions are identified	712/228

	Document ID	U	Title	Current OR
1	US 20030 16367 9 A1	<input type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
2	US 20030 13134 2 A1	<input type="checkbox"/>	Debugger with activity alert	717/125
3	US 65981 55 B1	<input type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
4	US 60063 16 A	<input type="checkbox"/>	Performing SIMD shift and arithmetic operation in non-SIMD architecture by operation on packed data of sub-operands and carry over-correction	712/22
5	US 58549 35 A	<input type="checkbox"/>	Program transformation system for microcomputer and microcomputer employing transformed program	717/159
6	US 58128 13 A	<input type="checkbox"/>	Apparatus and method for of register changes during execution of a micro instruction tracking sequence	712/218
7	US 57685 74 A	<input type="checkbox"/>	Microprocessor using an instruction field to expand the condition flags and a computer system employing the microprocessor	712/226
8	US 57519 85 A	<input type="checkbox"/>	Processor structure and method for tracking instruction status to maintain precise state	712/218
9	US 54817 05 A	<input type="checkbox"/>	Method for executing a program with branch-to modifying instructions	717/136
10	US 54737 43 A	<input type="checkbox"/>	Character generator with selectable conversion	345/471
11	US 54210 06 A	<input type="checkbox"/>	Method and apparatus for assessing integrity of computer system software	714/36
12	US 49721 31 A	<input type="checkbox"/>	Method of an apparatus for controlling velocity of industrial robot	318/568 .1
13	US 49185 93 A	<input type="checkbox"/>	Relational database system	707/200
14	US 41842 00 A	<input type="checkbox"/>	Integrating I/O element	713/200
15	US 35933 13 A	<input type="checkbox"/>	CALCULATOR APPARATUS	708/440

	Document ID	U	Title	Current OR
64	US 54169 13 A	<input checked="" type="checkbox"/>	Method and apparatus for dependency checking in a multi-pipelined microprocessor	712/216
65	US 53476 39 A	<input checked="" type="checkbox"/>	Self-parallelizing computer system and method	712/203
66	US 51519 91 A	<input checked="" type="checkbox"/>	Parallelization compile method and system	717/150
67	US 50880 34 A	<input checked="" type="checkbox"/>	Compiling method for determining programs to be executed parallelly by respective processors in a parallel computer which transfer data with a data identifier to other processors	717/160
68	US 50560 04 A	<input checked="" type="checkbox"/>	Program control system which simultaneously executes a program to be repeated and decrements repetition numbers	712/241
69	US 48435 40 A	<input checked="" type="checkbox"/>	Parallel processing method	712/11
70	US 48294 22 A	<input checked="" type="checkbox"/>	Control of multiple processors executing in parallel regions	718/106
71	US 48253 60 A	<input checked="" type="checkbox"/>	System and method for parallel processing with mostly functional languages	718/106
72	US 44981 36 A	<input checked="" type="checkbox"/>	Interrupt processor	710/262
73	US 44868 30 A	<input type="checkbox"/>	Programmable control apparatus and method	700/17
74	US 44123 03 A	<input checked="" type="checkbox"/>	Array processor architecture	712/16
75	US 43652 92 A	<input checked="" type="checkbox"/>	Array processor architecture connection network	712/14
76	US 43441 34 A	<input checked="" type="checkbox"/>	Partitionable parallel processor	712/16
77	US 41763 95 A	<input type="checkbox"/>	Interactive irrigation control system	700/284
78	US 37044 53 A	<input checked="" type="checkbox"/>	CATENATED FILES	710/21

	Document ID	U	Title	Current OR
1	US 20030 02875 7 A1	<input type="checkbox"/>	Concurrent modification and execution of instructions	712/226
2	US 66511 63 B1	<input checked="" type="checkbox"/>	Exception handling with reduced overhead in a multithreaded multiproCESSing system	712/244
3	US 65747 25 B1	<input checked="" type="checkbox"/>	Method and mechanism for speculatively executing threads of instructions	712/31
4	US 62021 99 B1	<input checked="" type="checkbox"/>	System and method for remotely analyzing the execution of computer programs	717/125
5	US 60525 28 A	<input checked="" type="checkbox"/>	Process for managing the multiple inheritance of persistent and shared objects	717/116
6	US 59997 34 A	<input checked="" type="checkbox"/>	Compiler-oriented apparatus for parallel compilation, simulation and execution of computer programs and hardware models	717/149
7	US 56946 04 A	<input checked="" type="checkbox"/>	Preemptive multithreading computer system with clock activated interrupt	718/107
8	US 56757 76 A	<input checked="" type="checkbox"/>	Data processor using FIFO memories for routing operations to parallel operational units	712/220
9	US 54148 22 A	<input checked="" type="checkbox"/>	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
10	US 53332 88 A	<input checked="" type="checkbox"/>	Effective address pre-calculation type pipelined microprocessor	711/214
11	US 45610 52 A	<input checked="" type="checkbox"/>	Instruction prefetch system	712/207
12	US 41093 11 A	<input checked="" type="checkbox"/>	Instruction execution modification mechanism for time slice controlled data processors	712/226
13	US 40842 35 A	<input checked="" type="checkbox"/>	Emulation apparatus	703/26
14	US 35933 13 A	<input checked="" type="checkbox"/>	CALCULATOR APPARATUS	708/440